

FIG. 1A
(PRIOR ART)

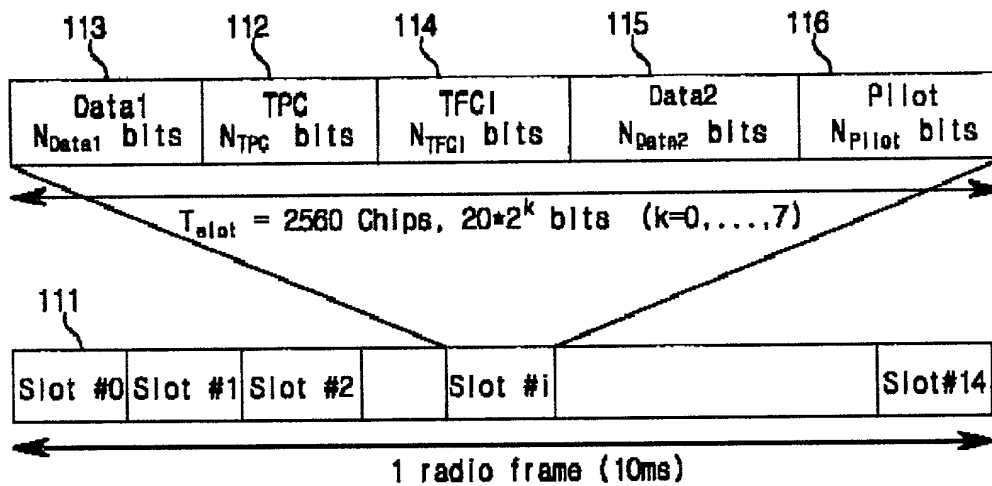


FIG. 1B
(PRIOR ART)

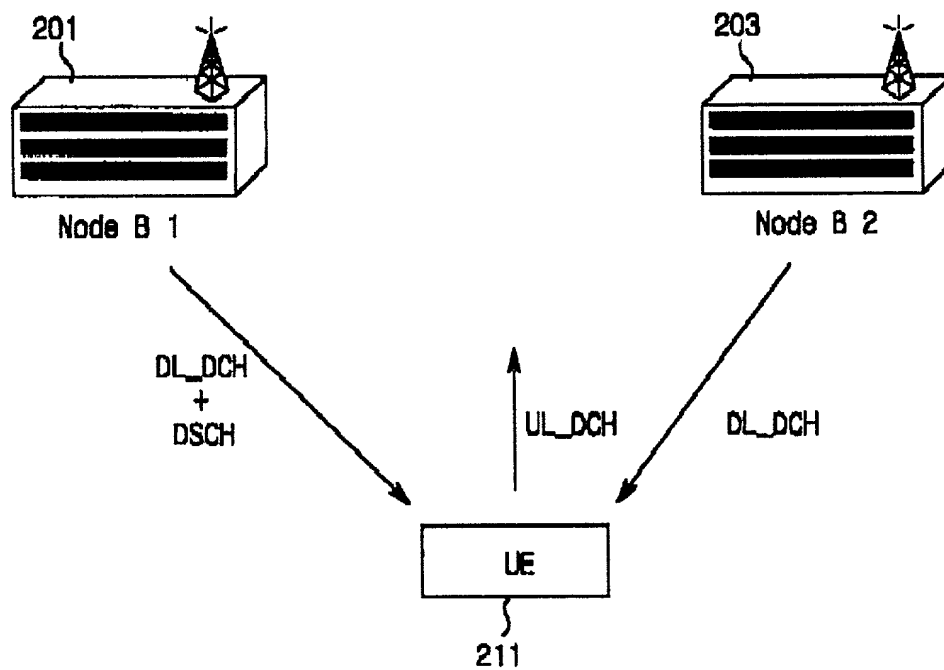


FIG. 2
(PRIOR ART)

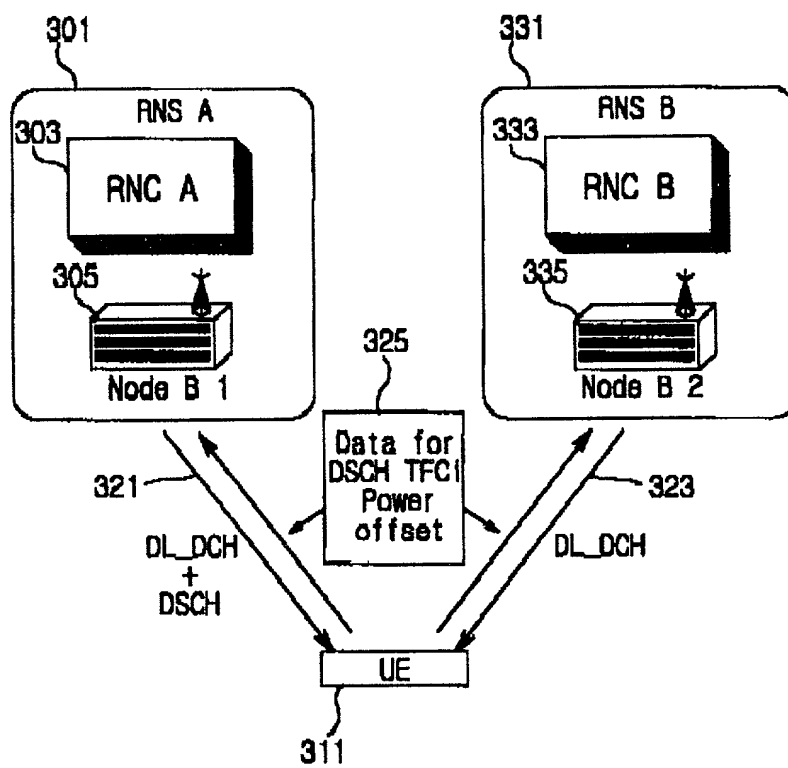


FIG. 3
(PRIOR ART)

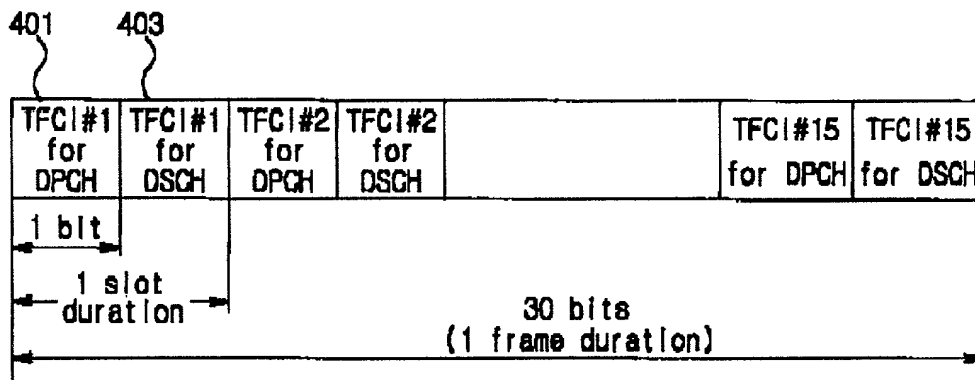


FIG. 4

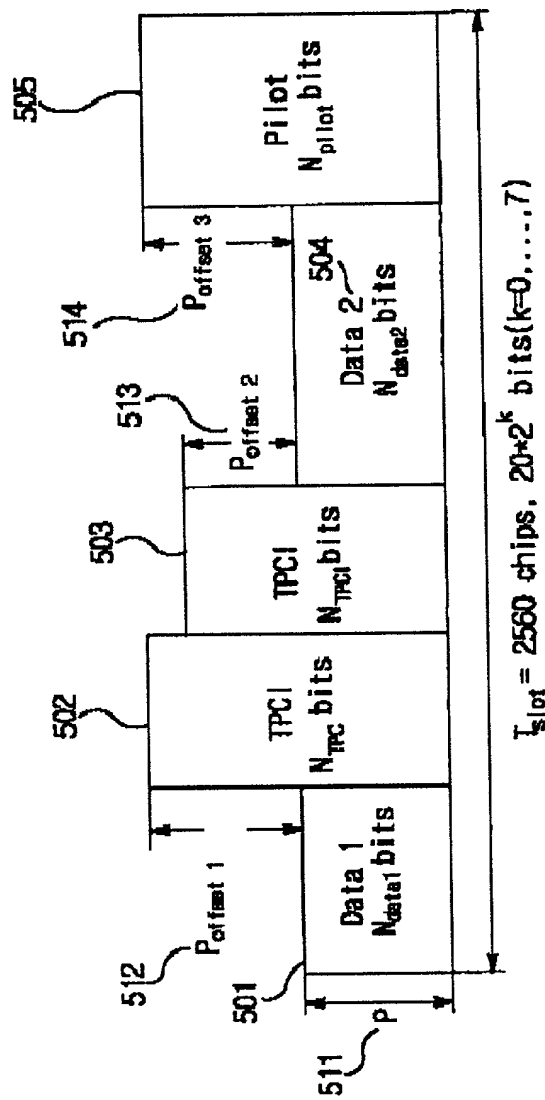


FIG. 5

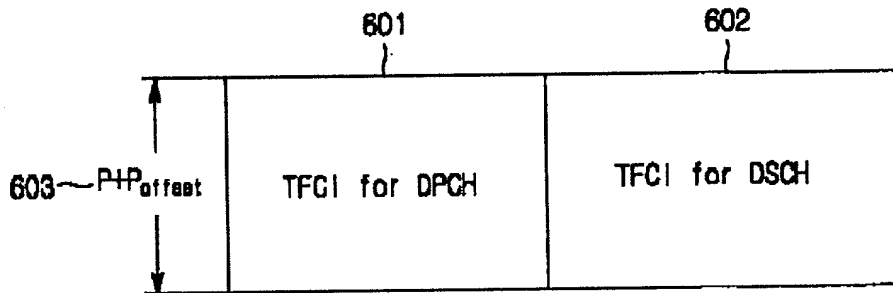


FIG. 6A

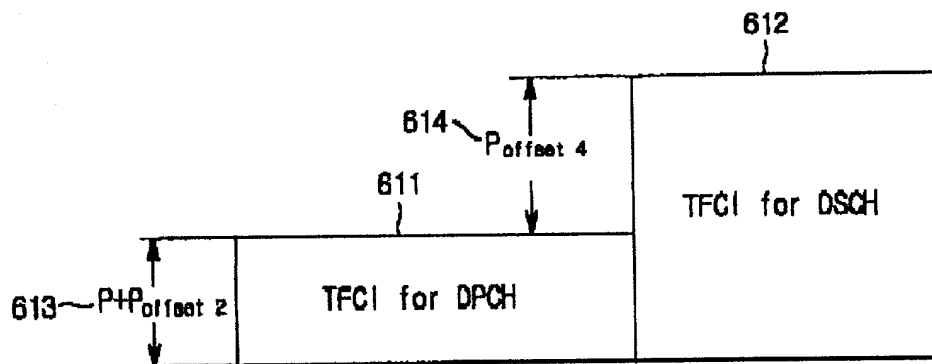


FIG. 6B

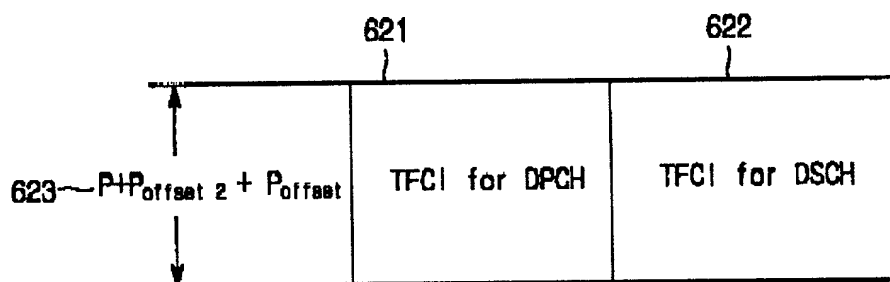


FIG. 6C

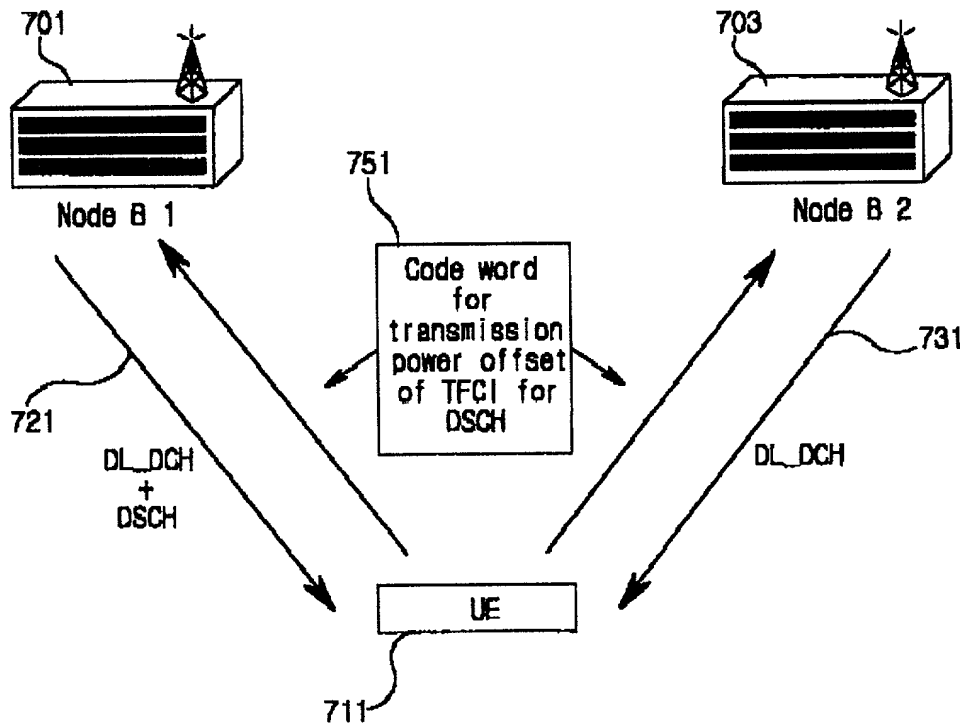


FIG. 7

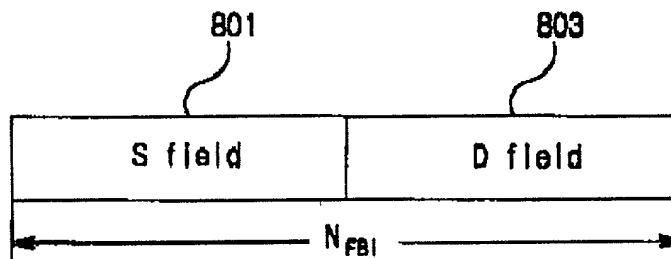


FIG. 8A

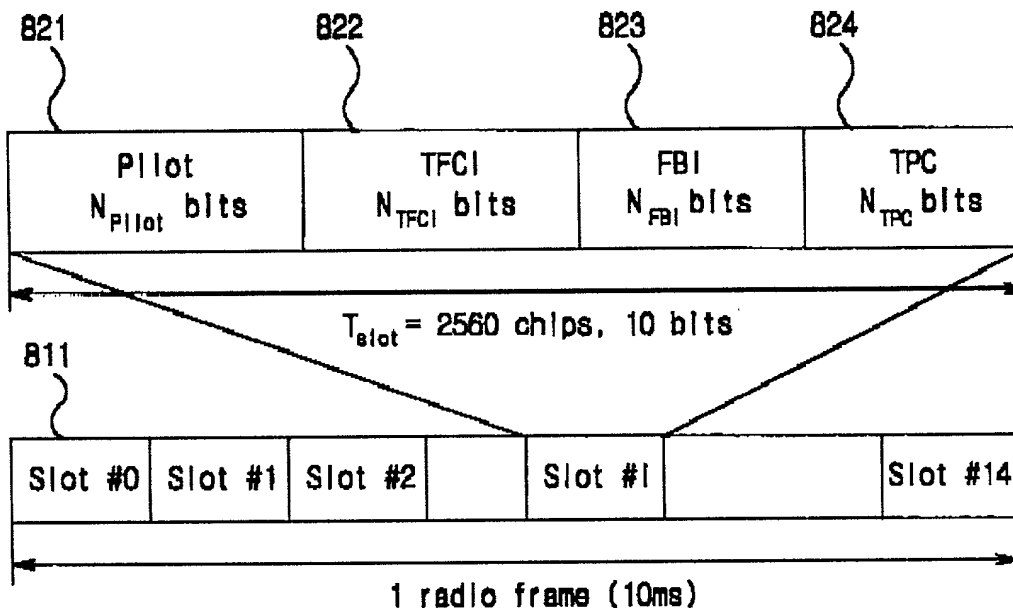


FIG. 8B

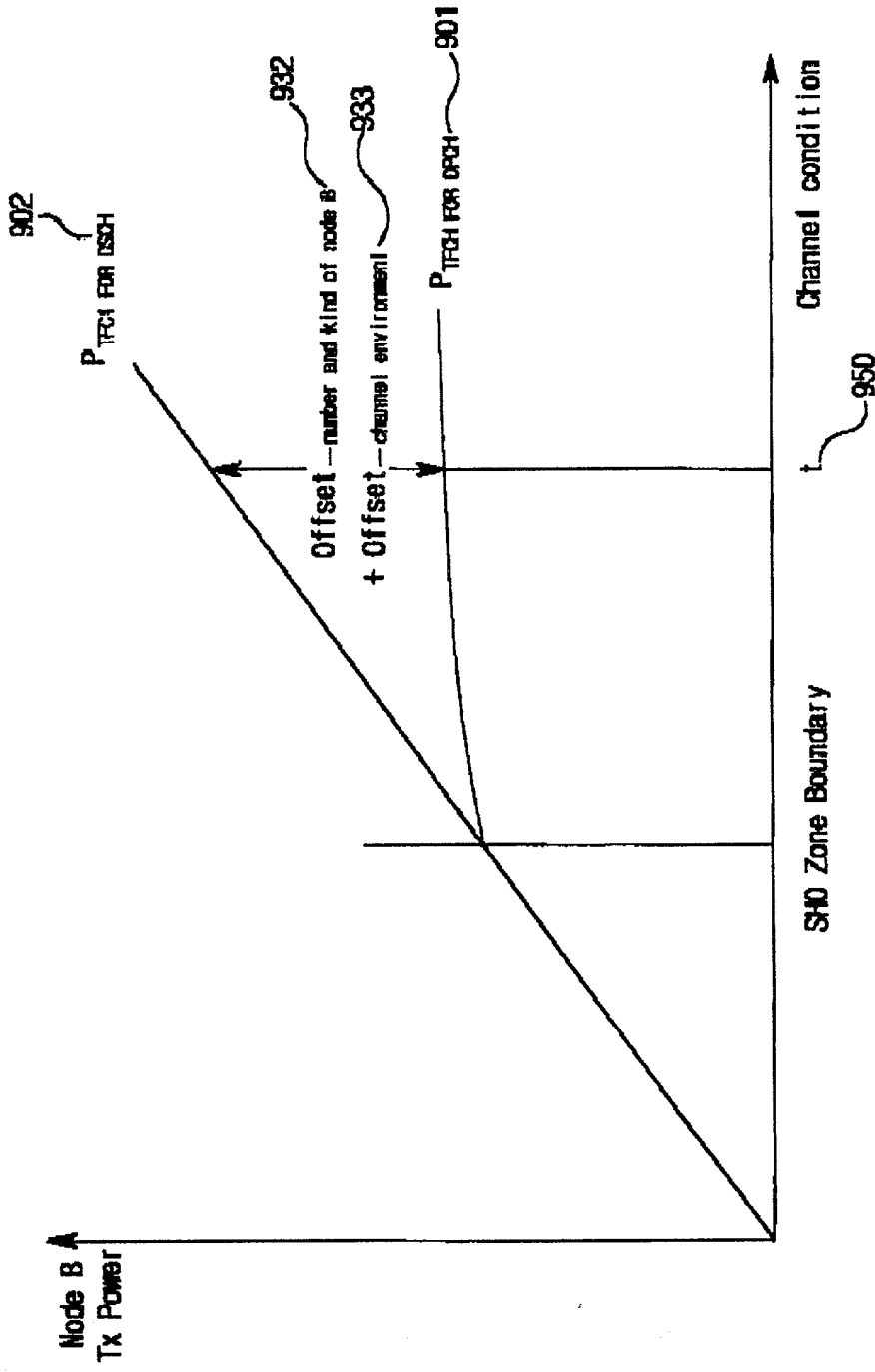


FIG. 9

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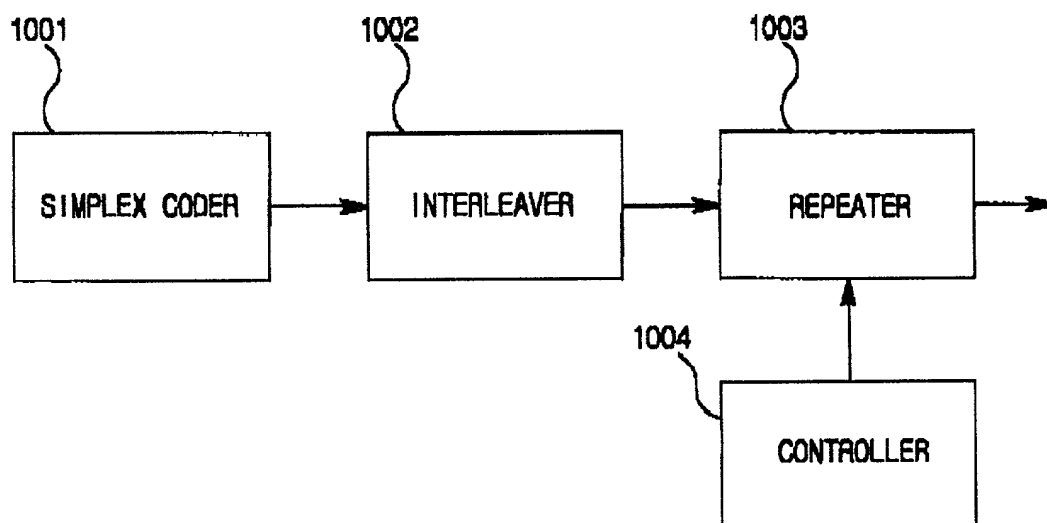


FIG. 10

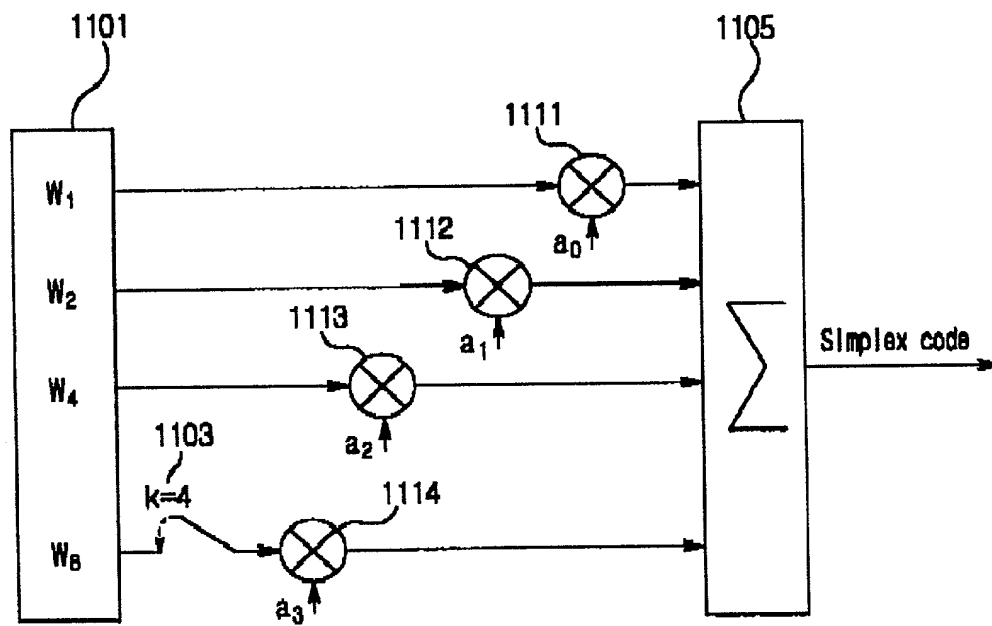


FIG. 11

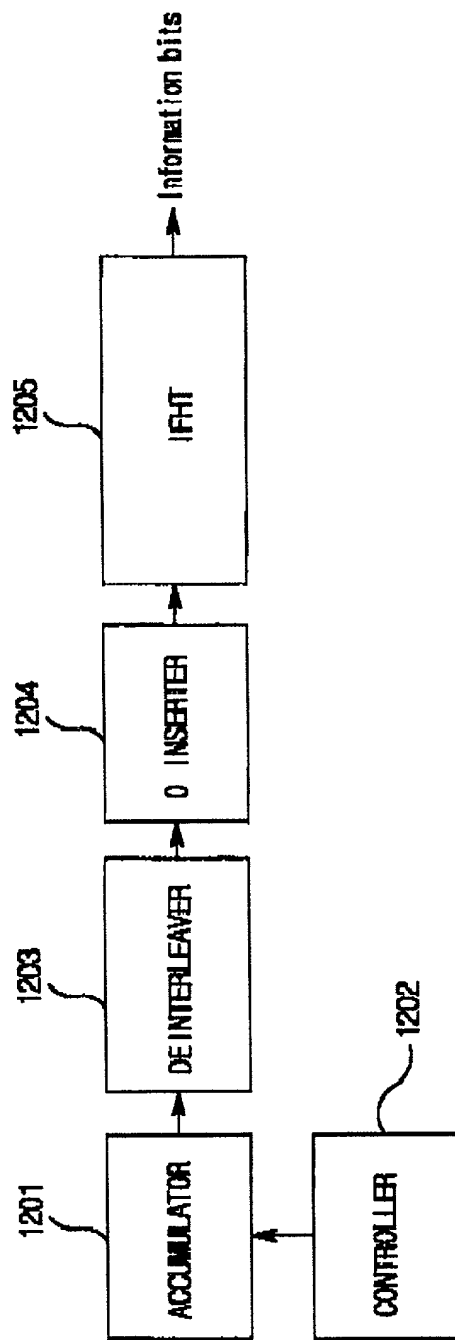


FIG. 12



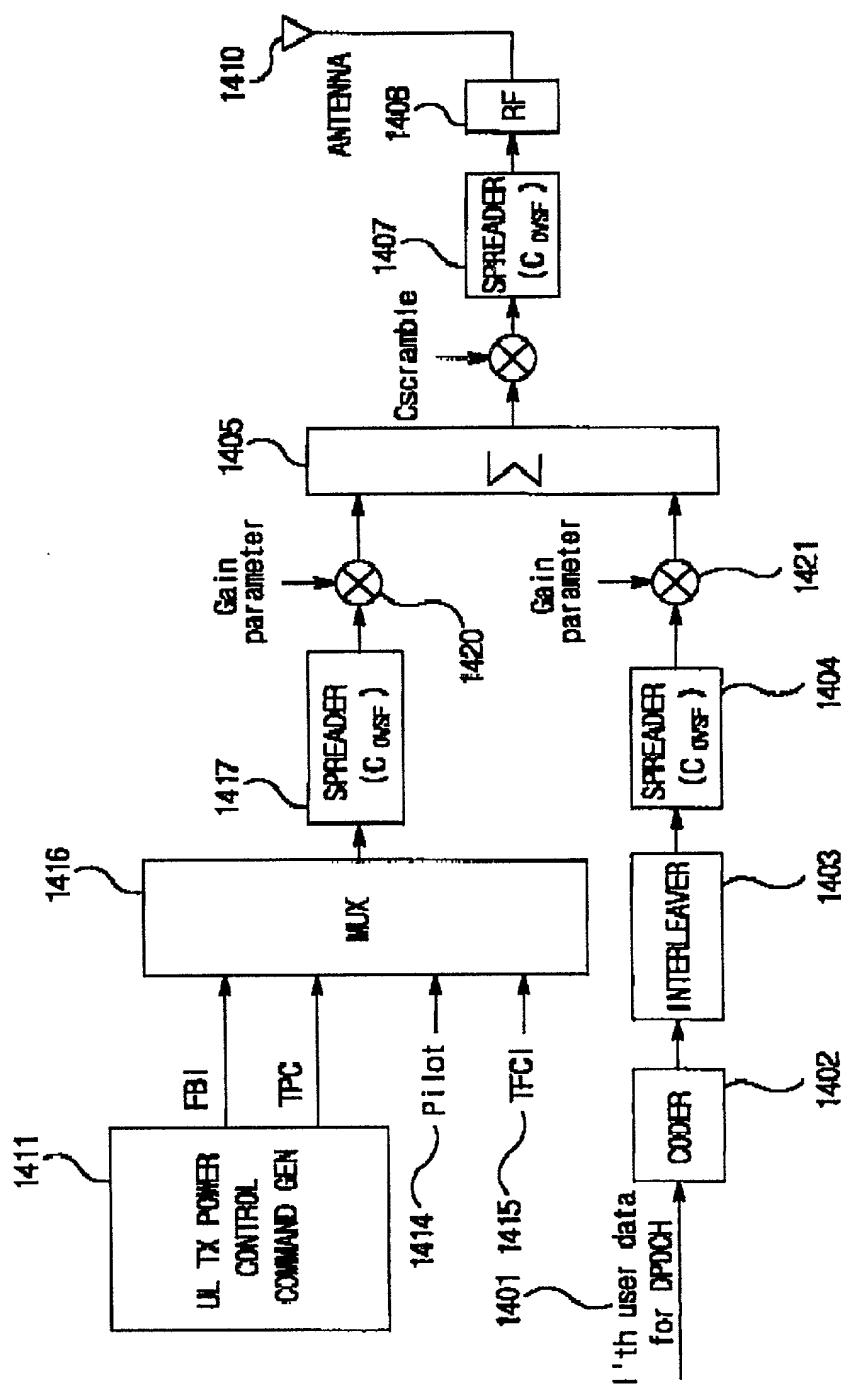


FIG. 14

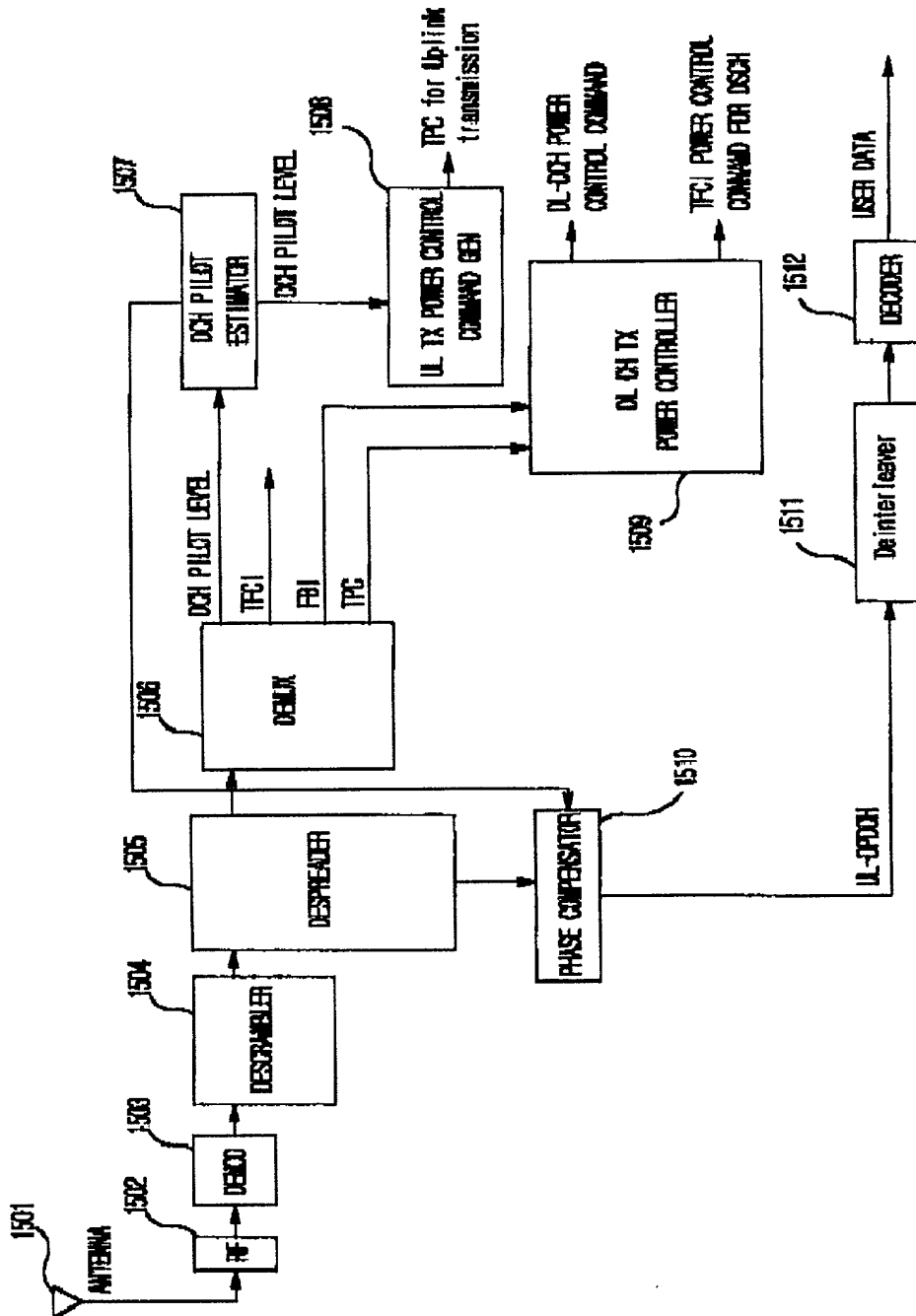


FIG. 15

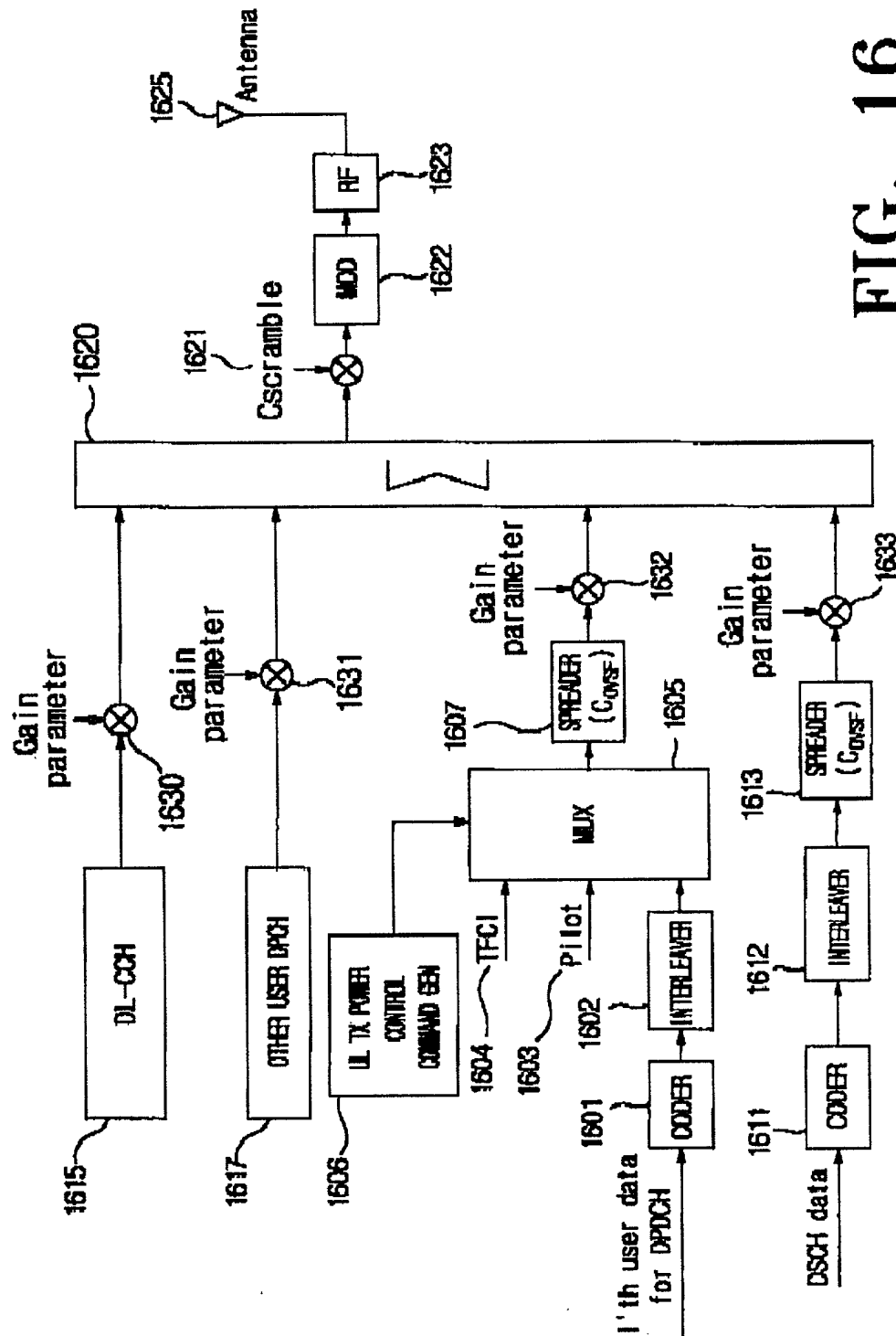


FIG. 16

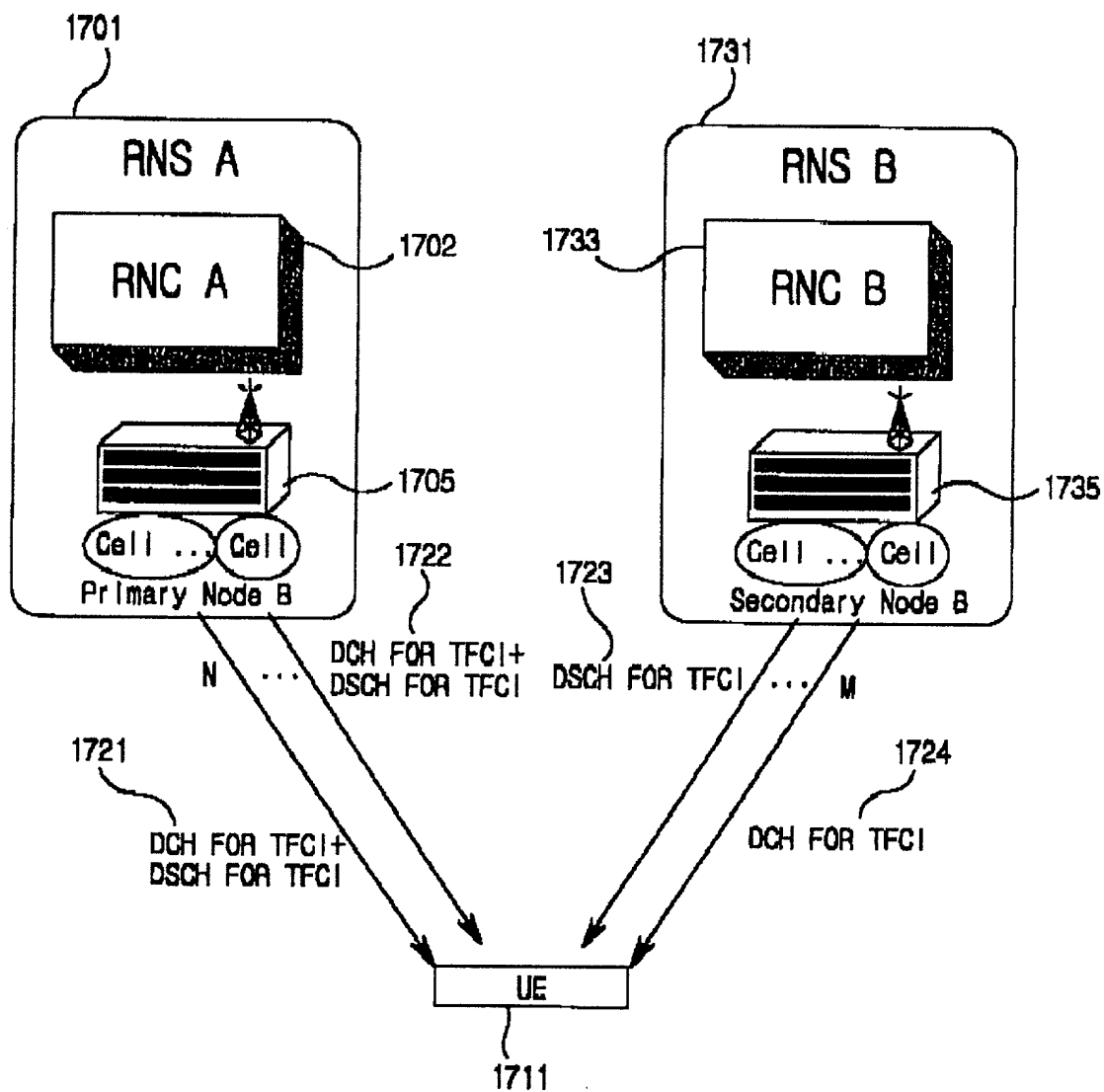


FIG. 17

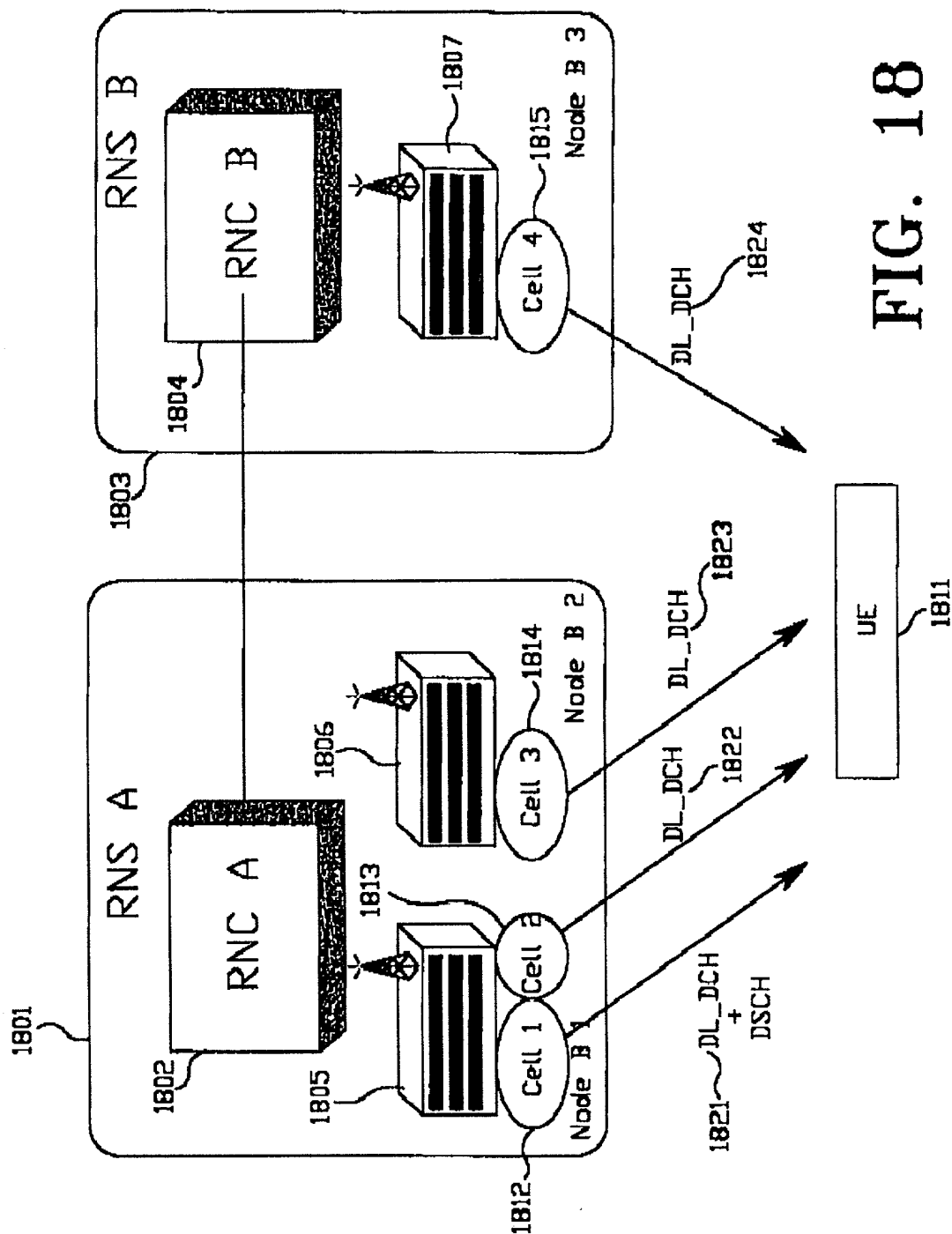


FIG. 18

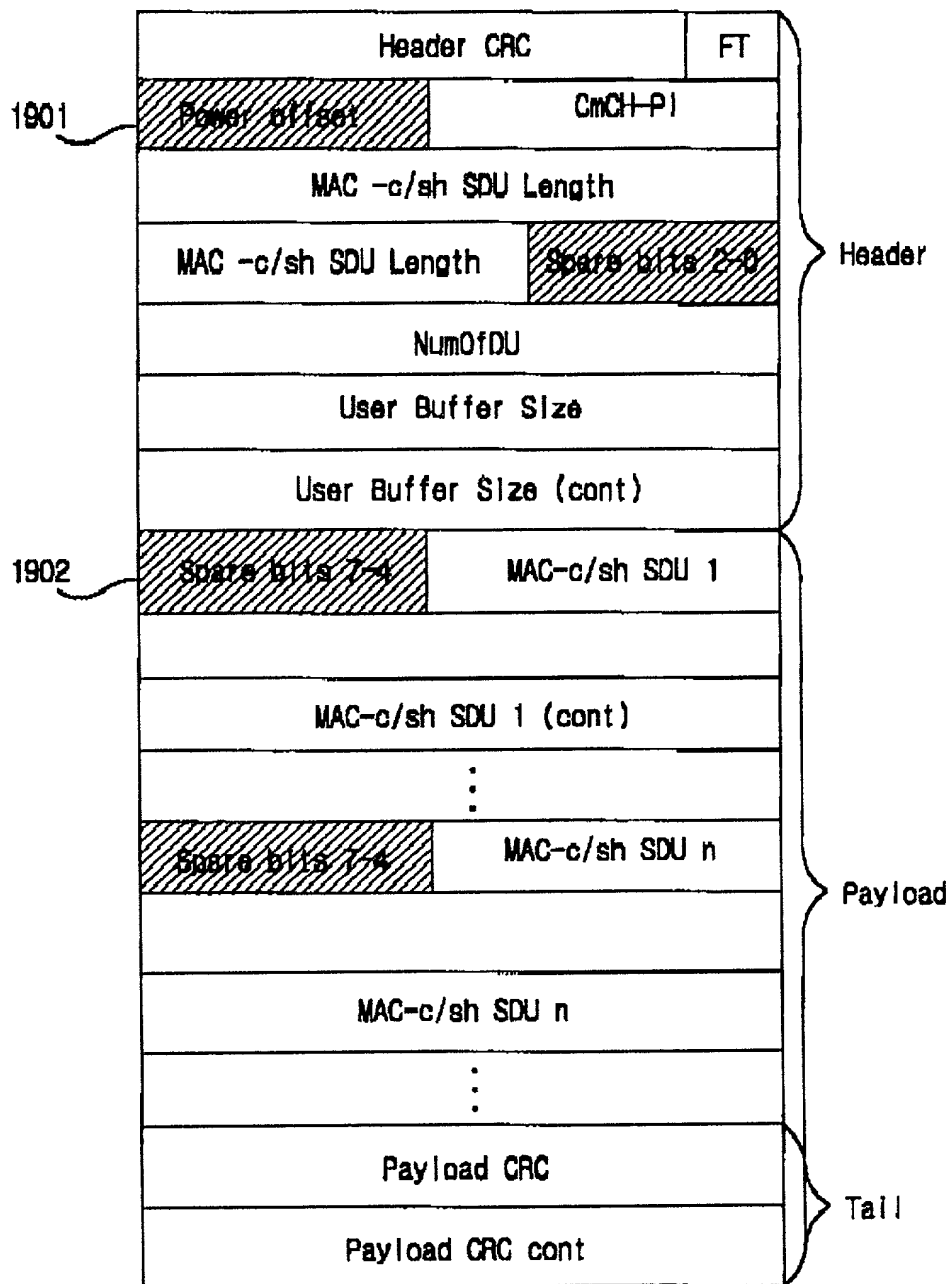


FIG. 19

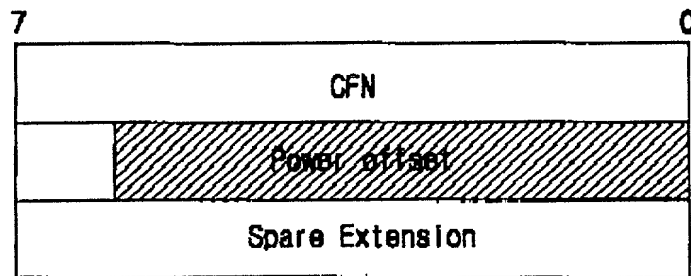
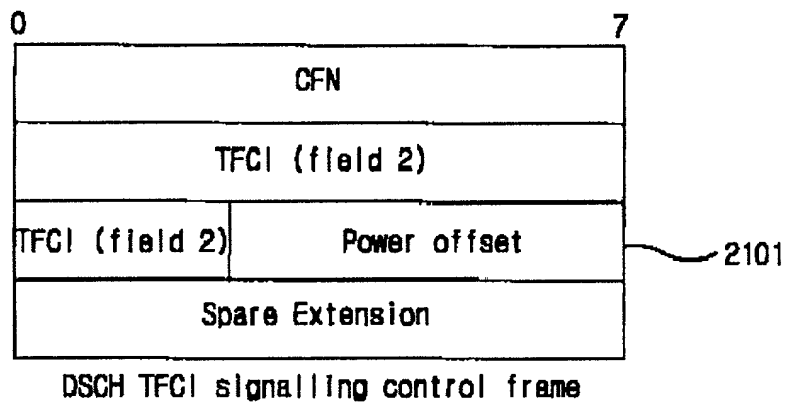


FIG. 20

**FIG. 21**

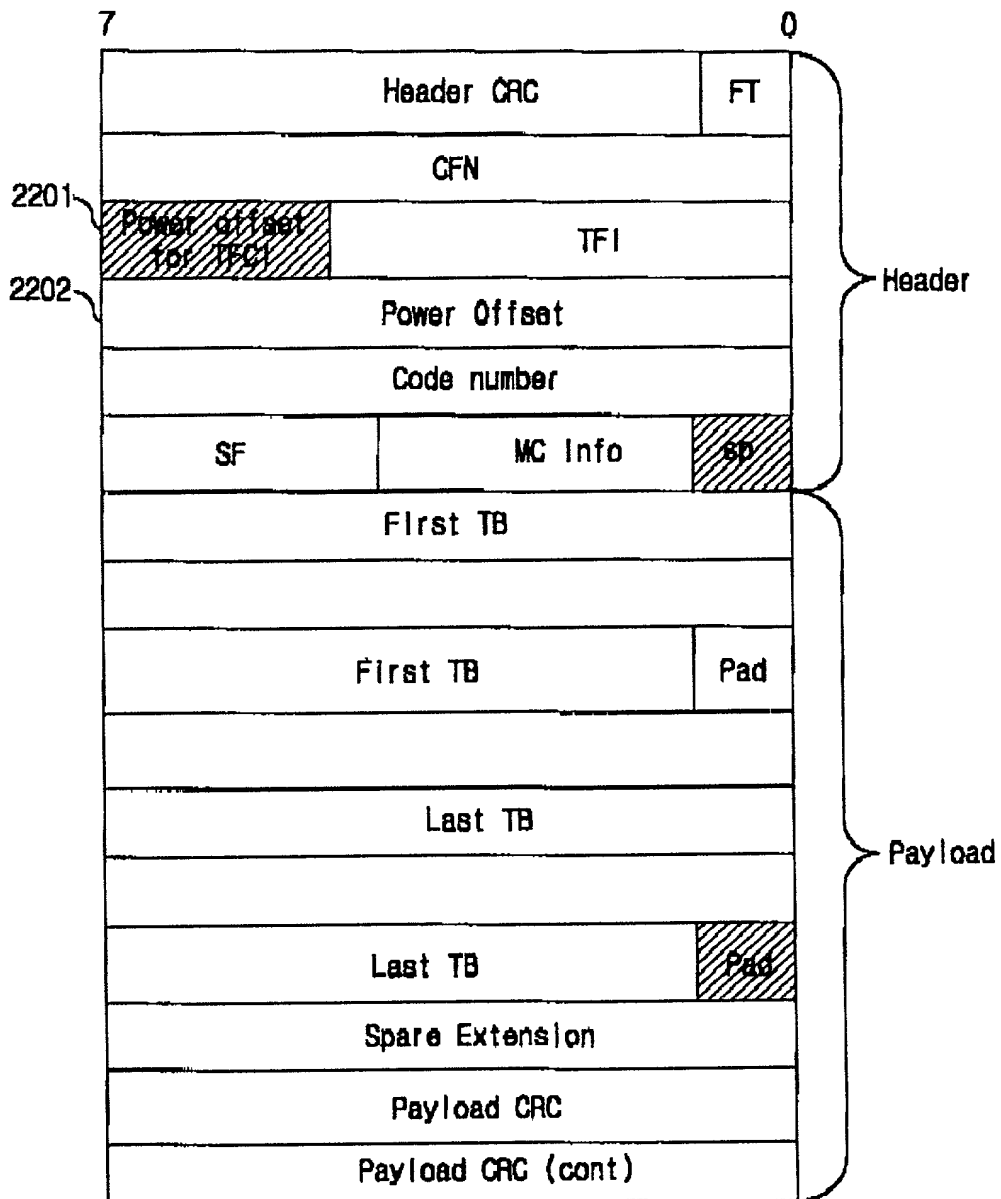


FIG. 22

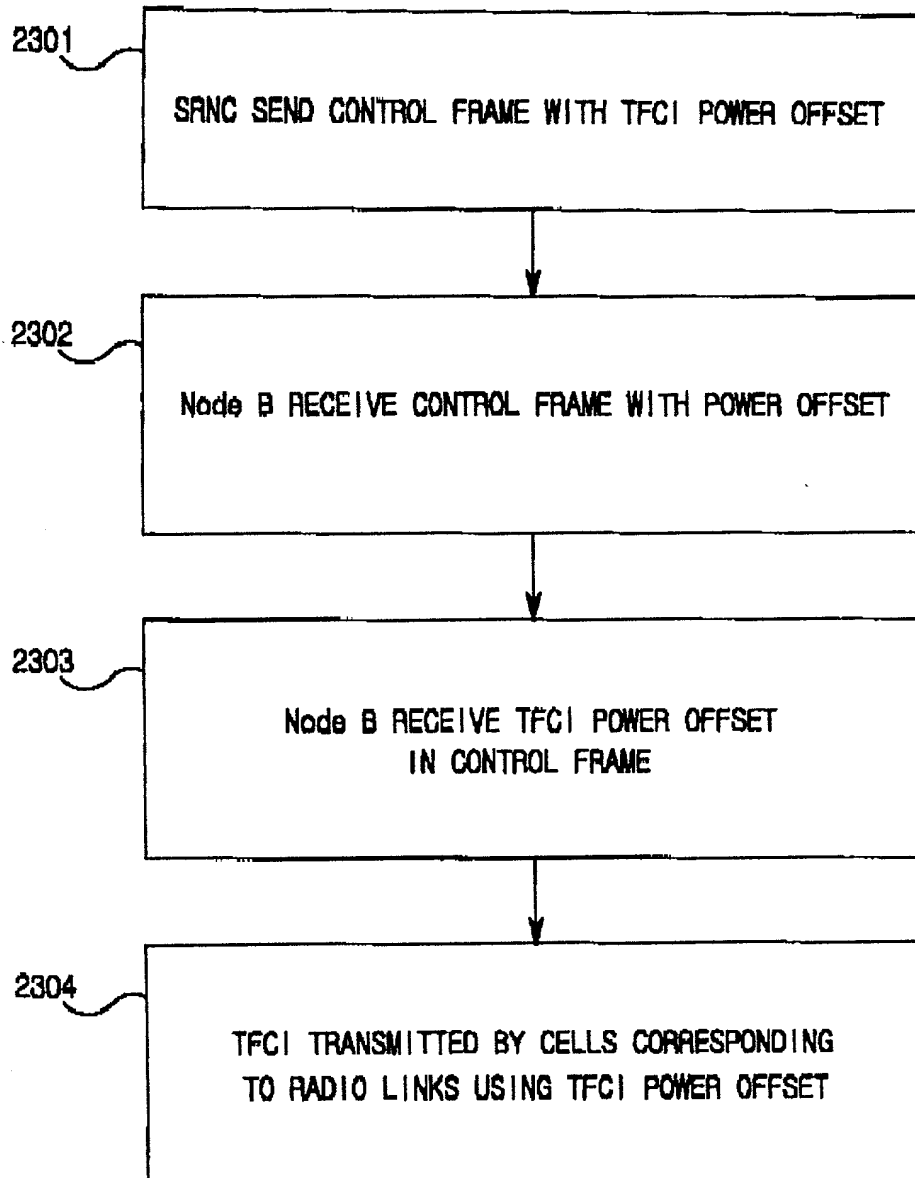


FIG. 23

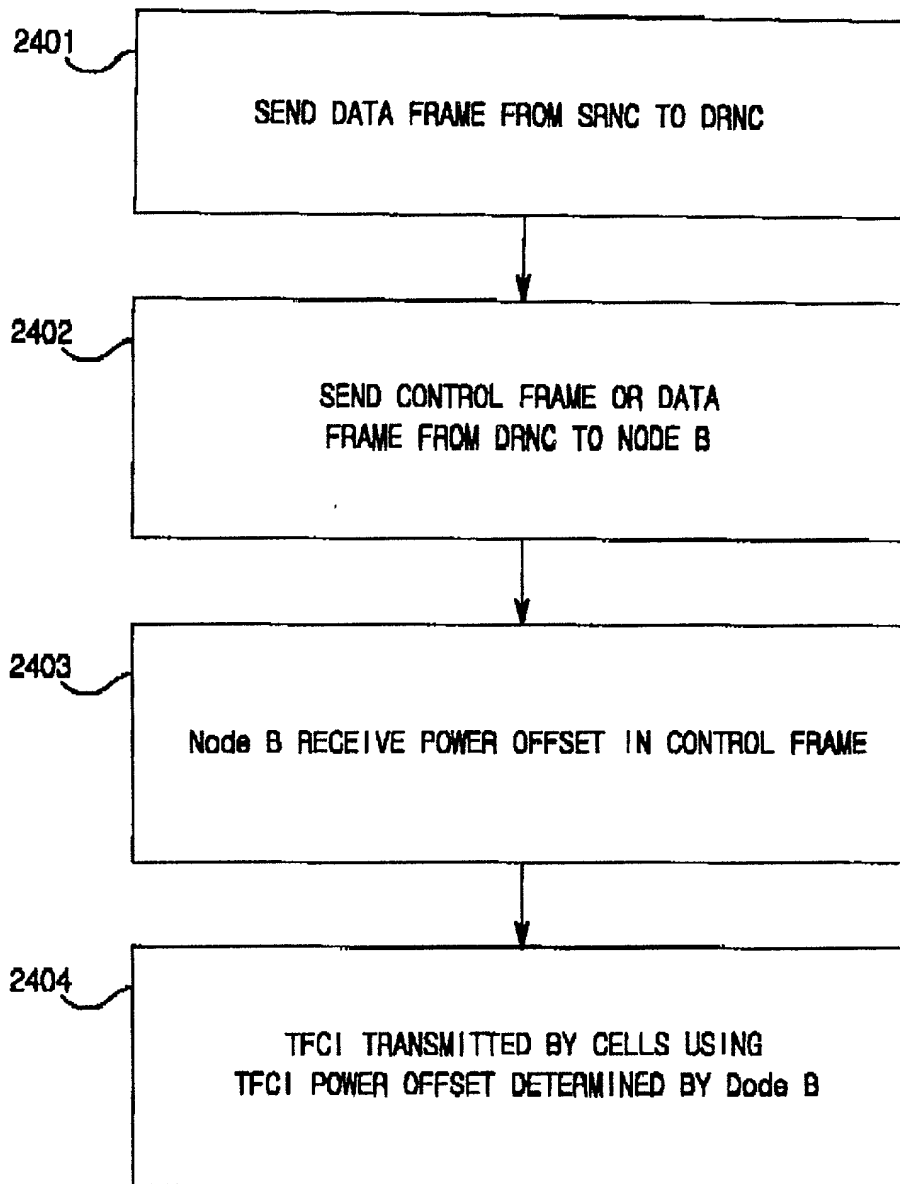


FIG. 24

9. 1.36 RADIO LINK SETUP REQUEST

9. 1.36. 1 FDD message

IE/Group Name	Presence	Range	IE type and reference	Semantics description	Criticality	Assigned criticality
Message Discriminator	M		9.2.1.45		—	
Message Type	M		9.2.1.46		YES	reject
CNDC Communication context ID	M		9.2.1.18		YES	reject
Transaction ID	M		9.2.1.62		—	
UL DPCCH Information		1			YES	reject
>UL Scrambling code	M		9.2.2.59		—	
>Min UL Channelisation Code Length	M		9.2.2.22		—	
>Max Number of UL DPCCHs	C - CodeLen		9.2.2.21		—	
>puncture limit	M		9.2.1.50	For UL	—	
>TFCS	M		9.2.1.58	For UL	—	
>UL DPCCH Slot Format	M		9.2.2.57		—	
>UL SIR Target	M		UL SIR 9.2.2.58		—	
>Diversity mode	M		9.2.2.9		—	
>SSDT cell ID Length	O		9.2.2.45		—	
>S Field Length	C-FBI		9.2.2.40		—	
DL DPCCH Information					YES	reject
>TFCS	M		9.2.1.58	For DL	—	
>DL DPCCH Slot Format	M		9.2.2.10		—	
>TFCI signalling mode	M		9.2.2.50		—	
>TFCI presence	C - SlotFormat		9.2.1.57		—	
>Multiplexing Position	M		9.2.2.29		—	
>PDSCH RLID	C-DSCH		RLID 9.2.1.53		—	
>PDSCH code mapping	C-DSCH		9.2.2.25		—	
>Power Offset Information		1			—	
>>P01	M		Power Offset 9.2.2.29	Power offset for the TFCI bits	—	
>>P02	M		Power Offset 9.2.2.29	Power offset for the TPC bits	—	
>>P03	M		Power Offset 9.2.2.29	Power offset for the pilot bits	—	
>FDD TPC DL Step Size	M		9.2.2.16		—	
The Rest Omitted						

FIG. 25

9. 1.36 RADIO LINK SETUP REQUEST

9. 1.36. 1 FDD message

IE/Group Name	Presence	Range	IE type and reference	Semantics description	Criticality	Assigned Criticality
Message Discriminator	M		9.2.1.45		—	
Message Type	M		9.2.1.46		YES	reject
CPNC Communication context ID	M		9.2.1.18		YES	reject
Transaction ID	M		9.2.1.62		—	
UL DPCCH Information		1			YES	reject
>UL Scrambling code	M		9.2.2.59		—	
>Min UL Channelisation Code Length	M		9.2.2.22		—	
>Max Number of UL DPCCHs	C - CodeLen		9.2.2.21		—	
>puncture limit	M		9.2.1.50	For UL	—	
>TFCS	M		9.2.1.58	For UL	—	
>UL DPCCH Slot Format	M		9.2.2.57		—	
>UL SIR Target	M		UL SIR 9.2.2.58		—	
>Diversity mode	M		9.2.2.9		—	
>SSOT cell ID Length	O		9.2.2.45		—	
>S Field Length	C-FBI		9.2.2.40		—	
DL DPCCH Information					YES	reject
>TFCS	M		9.2.1.58	For DL	—	
>DL DPCCH Slot Format	M		9.2.2.10		—	
>TFCI signalling mode	M		9.2.2.50		—	
>TFCI presence	C - SlotFormat		9.2.1.57		—	
>Multiplexing Position	M		9.2.2.29		—	
>PDSCH RLIO	C-DSCH		RL ID 9.2.1.53		—	
>PDSCH code mapping	C-DSCH		9.2.2.25		—	
>Power Offset Information		1			—	
>>P01	M		Power Offset 9.2.2.29	Power offset for the TFCI bits	—	
>>P02	M		Power Offset 9.2.2.29	Power offset for the TPC bits	—	
>>P03	M		Power Offset 9.2.2.29	Power offset for the pilot bits	—	
>>P04	M		9.2.2.29	Power offset for the TFCI bits for DSCH	—	

The Rest Omitted

FIG. 26

9. 1.47 RADIO LINK RECONFIGURATION FRQUEST

9. 1.47. 1 FDD message

IE/Group Name	Presence	Range	IE type and Reference	Semantics Description	Criticality	Assigned Criticality
Message Discriminator	M		9.2.1.45		—	
Message Type	M		9.2.1.46		YES	reject
Node B Communication Context ID	M		9.2.1.48	The reserved value "ALL NBCC" shall not be used.	YES	reject
Transaction ID	M		9.2.1.62		—	
UL DPCCH Information		0..1			YES	reject
>TFCS	○		9.2.1.58	For the UL.	—	
DL DPCCH Information		0..1			YES	reject
>TFCS	○		9.2.1.58	For the UL.		
>TFCI Signalling Mode	○		9.2.2.50		—	
>Limited Power Increase	○					
>Power Offset Information		1			—	
>>P01	M		Power Offset 9.2.2.29	Power offset for the TFCI bits	—	
>>P04	M		Power Offset 9.2.2.29	Power offset for the TFCI bits for DSCH	—	

The Rest Omitted

FIG. 27